REMARKS

Claims 1-26 are pending in the application. In response to the office action, applicants have amended claims 9 and 18. Claims 1-26 remain pending for reconsideration.

Applicants note that the present response is accompanied by a petition to revive the application and a Request for Continued Examination (RCE).

Claims 1-3, 9-12, 16-21, and 25-26 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,987,538 (Tavallaei). Applicants respectfully traverse this rejection for the following reasons.

In order to anticipate, the reference must identically disclose each claim element. In fact, Tavallaei does not identically disclose many of the recited claim elements.

The office action asserts that component 14 in Figure 2 of Tavallaei corresponds to the recited scaleable node controllers. However, Tavallaei describes component 14 as a local advanced programmable interrupt controller (APIC). A local APIC is not identical to a scaleable node controller.

In the Examiner's response to arguments, at numbered paragraph 55, the Examiner acknowledges that the terminology is different but asserts that the different terminology is irrelevant because the local APIC 14 performs the same function as the recited scaleable node controller. This is simply incorrect. The different terminology in fact describes different structure and functionality. Every 'controller' does not perform the same function as every other 'controller'. One skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. Moreover, one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. For example, a node controller may have suitable structure to participate in an interrupt

handling scheme, but an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

The office action asserts that component 26 in Figure 2 of Tavallaei corresponds to the recited scalability port switch. However, Tavallaei describes component 26 as an external input / output advanced programmable interrupt controller (I/O APIC). An I/O APIC is not identical to a scalability port switch.

In the Examiner's response to arguments, at numbered paragraph 55, the Examiner acknowledges that the terminology is different but asserts that the different terminology is irrelevant because the I/O APIC 26 performs the same function as the recited scalability port switch. This is simply incorrect. The different terminology in fact describes different structure and functionality. Every 'I/O' controller does not perform the same function as every other I/O switch. One skilled in the art would appreciate that a port switch performs a different function than an I/O interrupt controller. Moreover, one skilled in the art would appreciate that a port switch has a different structure from an I/O interrupt controller. For example, a port switch may have suitable structure to participate in an interrupt handling scheme, but an I/O interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. For example, in some applications a port switch may include structure to resolve node addresses. The I/O APIC 26 appears to lack such structure.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Tavallaei fails to teach or suggest this further recitation. In contrast to the present invention, Tavallaei describes a multi-processor system with local APICs 14 connected to the I/O APIC 26 over the APIC bus 16. Tavallaei describes that the I/O APIC 26 generates an interrupt message on the APIC bus 16, which is monitored by all the local APICs 14. The local APICs 14 appear to be responsive to the content of the interrupt messages for passing on local interrupts for the associated processor 12. The Examiner has not identified (and applicants

are unable to identify) any portion of Tavallaei that teaches or suggests that the local APICs 14 have addresses associated therewith.

In the Examiner's response to arguments, at numbered paragraph 56, the Examiner appears to be relying on a theory of inherency. In other words, the Examiner appears to be arguing that because the message is received by the appropriate local APIC 14, the local APIC 14 inherently must have an address associated therewith. However, this is incorrect. Any of a number of schemes may be utilized for getting messages to the appropriate processor 12. For example, the processor 12 in Tavallaei may include a processor ID and the message on the APIC bus 16 may include the processor ID. Tavallaei expressly describes that the APIC 26 maintains a table that indicates "which of the processors 12 the interrupt is to be directed." (see col. 7, lines 43-44, emphasis added). The fact of the matter is that Tavallaei is completely silent with respect to any address associated with the local APIC 14. In order to clarify issues for possible appeal, the Examiner should admit that Tavallaei does not expressly teach the recited addresses and set forth the Examiner's position with respect to inherency (particularly the Examiner's technical argument for how such addresses are allegedly the only possible way to deliver data from the I/O APIC 26 to the local APIC 14).

Because Tavallaei fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Tavallaei, and is patentable over Tavallaei. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Tavallaei does not disclose the recited scaleable node controller or the recited scalability port switch. Claims 9 and 18 have been amended to clarify that determining the scaleable node controller includes determining an address of the scaleable node controller. For the reasons given above Tavallaei does not disclose determining an address of the local APIC 14. Accordingly, claim 9 and its dependent claims 10-12 and 16-17 are not anticipated by and are patentable over Tavallaei. Likewise, claim 18 and its dependent claims 19-21 and 25-26 are patentable over Tavallaei.

With respect to claims 11 and 20, the office action identifies col. 7 lines 41-44 for the recited comparing a priority of the interrupt request with a priority of the processor. However, the cited portion makes no reference whatsoever to a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei.

In the Examiner's response to arguments, at numbered paragraph 58, the Examiner sets forth a position which still fails to address the fact that Tavallaei does not disclose any priority of the processor. Assuming, for the sake of argument, that the Examiner is correct that the reference discloses 1) priorities associated with interrupts and 2) which processor an interrupt is directed to, it does not follow that Tavallaei discloses anything whatsoever with respect to the priority of the processor. The fact of the matter is that Tavallaei does not describe a priority associated with the processor 12 or comparing the priority of the interrupt with a priority of a processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei. The Examiner is respectfully requested to answer this specific traversal.

Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig). Applicants respectfully traverse this rejection for the following reasons.

In order to anticipate, the reference must identically disclose each claim element. In fact, Olarig does not identically disclose many of the recited claim elements.

The office action asserts that components 107 and 306 in Figure 4 of Olarig correspond to the recited scaleable node controllers. However, Olarig describes component 107 as a cache and component 306 as a local programmable interrupt controller (LOPIC). A cache and a LOPIC are not identical to a scaleable node controller.

In the Examiner's response to arguments, in numbered paragraph 59, the Examiner acknowledges that the terminology is different but asserts that the different terminology is irrelevant because the cache 107 and LOPIC 306 perform the same function as the recited

scaleable node controller. This is simply incorrect. The different terminology in fact describes different structure and functionality. A cache has no relationship whatsoever in structure or functionality to a node controller. With respect to the LOPOC 306, every 'controller' does not perform the same function as every other 'controller'. One skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. Moreover, one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. For example, a node controller may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

The office action asserts that component 312 in Figure 4 of Olarig corresponds to the recited scalability port switch. However, Olarig describes component 312 as a central programmable interrupt controller (COPIC). A COPIC is not identical to a scalability port switch.

In the Examiner's response to arguments, at numbered paragraph 59, the Examiner acknowledges that the terminology is different but asserts that the different terminology is irrelevant because the COPIC 312 performs the same function as the recited scalability port switch. This is simply incorrect. The different terminology in fact describes different structure and functionality. Every controller does not perform the same function as every other controller. One skilled in the art would appreciate that a port switch performs a different function than an interrupt controller. Moreover, one skilled in the art would appreciate that a port switch has a different structure from an interrupt controller. For example, a port switch may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. For example, in some applications a port switch may include structure to resolve node addresses. The COPIC 312 appears to lack such structure.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Olarig fails to teach or suggest this further recitation. In contrast to the present invention, Olarig describes a multi-processor system with LOPICs 306 connected to the COPIC 312 over the PIC bus 311. Olarig appears to function similarly to Tavallaei as discussed above. The Examiner has not identified (and applicants are unable to identify) any portion of Olarig that teaches or suggests that the LOPICs 306 have addresses associated therewith.

In the Examiner's response to arguments, at numbered paragraph 60, the Examiner appears to be relying on a theory of inherency. In other words, the Examiner appears to be arguing that because data is received by the LOPIC 306, the LOPIC 306 inherently must have an address associated therewith. However, this is incorrect. Any of a number of schemes may be utilized for getting data to the appropriate processor 106. For example, the processor 106 in Olarig may include a processor ID and the message on the bus 311 may include the processor ID. Oarig expressly describes that the LOPIC maintains a register with the processor ID and the processor ID is used for delivering interrupts (see col. 7, lines 46-51). The fact of the matter is that Olarig is completely silent with respect to any address associated with the LOPIC 306. In order to clarify issues for possible appeal, the Examiner should admit that Olarig does not expressly teach the recited addresses and set forth the Examiner's position with respect to inherency (particularly the Examiner's technical argument for how such addresses are allegedly the only possible way to deliver data from the COPIC 312 to the LOPIC 306).

Because Olarig fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Olarig, and is patentable over Olarig. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Olarig does not disclose the recited scaleable node controller, the recited scalability port switch, or the recited address of the scaleable node controller. Accordingly, claim 9 and its dependent claims 10-12 and

14-17 are not anticipated by and are patentable over Olarig. Likewise, claim 18 and its dependent claims 19-21 and 23-26 are patentable over Olarig.

With respect to claims 11 and 20, the office action identifies col. 10, lines 8-10 for the recited comparing a priority of the interrupt request with a priority of the processor. In the Examiner's response to arguments, in numbered paragraph 61, the Examiner further identifies col. 3, lines 4-7 for this recitation. Col. 3, lines 4-7 discusses only comparing the priority of the interrupt with priorities of other tasks. Col. 10, lines 8-10 (which has no connection with the other cited portion of col. 3, lines 4-7) discusses only comparing a processor task priority level with other processors to select the least busy processor. However, neither cited portion makes any reference whatsoever to comparing a priority of the interrupt request with a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Olarig. . The Examiner is respectfully requested to answer this specific traversal.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal). Applicants respectfully traverse this rejection for the following reasons.

Neal fails to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness.

Moreover, claim 4 recites a first input/output hub coupled between the peripheral component interconnect bus and the first scalability port switch, wherein said first input/output hub is able to support a plurality of additional peripheral component interconnect hubs. The office action asserts that component 28 corresponds to the recited hub. However, component 28 is simply described as an ASIC connected to a PCI bus, not an I/O hub. In fact, the word "hub" cannot be found in Tavallaei. No one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal.

In numbered paragraph 62, the Examiner yet again fails to give different terminology any relevance, even though the different terms in fact refer to different structures. One of ordinary skill in the art would appreciate that the ASIC 28 does not necessarily have the same structure or perform the same function as an I/O hub, just because it is attached to a PCI bus.

Because the office action fails to establish a prima facie case of obviousness and because the ASIC 28 is not an I/O hub, claim 4 is patentable over Tavallaei in view of Neal. Claim 5 depends from claim 4 and is likewise patentable.

Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Olarig. Applicants respectfully traverse this rejection for the following reasons.

Neal and Olarig both fail to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness. Claim 6 and 7 depend from claim 5, and are accordingly patentable for the reasons given above. Claims 6 and 7 are further patentable for the following reasons.

Claim 6 recites that the first pair of scaleable node controllers and the second pair of scaleable node controllers are coupled to a second scalability port switch. Claim 7 depends from claim 6 and further recites that the second scalability port switch is coupled to the first input/output hub. Each of Tavallaei and Olarig describe that the respective local APICs 14 and the LOPICs 306 are closely associated with a single processors, identifying and handling interrupts for only the closely associated processor. Olarig does not suggest the type of interconnectivity recited in the claims. The multiple COPICs mentioned in Olarig appear to relate to a hierarchically distributed interrupt handling arrangement, and not to any LOPIC being coupled to more than one COPIC.

In the Examiner's response to arguments, in numbered paragraph 63, the Examiner baldy asserts that the references teach the recitation of claims 6-7 without clarifying the Examiner's position. The Examiner incorrectly cites Figure 2 of Tavallaei, which discloses

only a single I/O ASIC 26. The Examiner incorrectly cites Figure 4 of Olarig, which discloses only a single COPIC 312. The Examiner again cites col. 8, lines 5-13 (which actually refers to Fig. 3, not Fig. 4). The relied upon portion reads "[a]lthough only one COPIC 312 is shown in this embodiment, it can be readily understood upon reference hereto that a plurality of central programmable interrupt controllers may be utilized within the scope of the present invention." The cited portion does not teach or suggest that the LOPICs 306 would be cross-connected with each of the COPICs 312. It merely describes that the LOPICs 306 may be subdivided among a plurality of COPICs 312. In other words, instead of eight LOPICs 306 being connected to one COPIC 312, other embodiments may utilize two COPICs 312 with four LOPICs 306 connected to each COPIC 312.

Because the office fails to establish a prima facie case of obviousness and because Olarig does not teach or suggest two pair of scaleable node controllers with each pair connected to two different scalability port switches, claims 6 and 7 are separately patentable over Tavallaei in view of Neal and further in view of Olarig.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, further in view of Olarig, and further in view of U.S. Patent No. 6,606,676 (Deshpande). Applicants respectfully traverse this rejection for the following reasons.

None of the secondary references make up for the missing teachings of Tavallaei noted above. For example, none of the cited references even mentions a scalability port switch. Therefore, the office action fails to establish a prima facie case of obviousness. Moreover, the office action fails to provide legally sufficient motivation to combine or modify the references in the manner suggested. The office action appears to use the claims as a blueprint to pick and choose pieces of prior art which allegedly read on various claim recitations without identifying any portion of the references which actually suggests the desirability of any of the proposed modifications. In particular, no one skilled in the art would be motivated to combine the multiplicity of references as applied in the rejection of claim 8, absent the teachings of the present application.

In particular, the office action suggests modifying Tavallaei to have multiple processors connected to the local APIC 14. This is simply unworkable. The local APICs are dedicated to the local processors 12, which Tavallaei describes as preferably being located on the same chip (see col. 6, lines 9-13). No one skilled in the art would be motivated to modify Tavallaei in the manner proposed in the office action. The Examiner is respectfully requested to answer this specific traversal.

The office action asserts that the combination of four references is obvious "because it would reduce traffic on the bus shared between the nodes." However, this motivation is completely contrived and provided without basis or explanation of the Examiner's position. If the rejection is maintained, applicants respectfully request that the Examiner identify every element of Tavallaei which is proposed to be modified and the textual or other basis which suggests making such modification. The Examiner is respectfully requested to answer this specific traversal.

In the Examiner's response to arguments, in numbered paragraph 64, the Examiner cites an irrelevant legal proposition. First, applicants have not even argued about the excessive number of references (although it is notable). The cited proposition qualifies itself with the phrase 'without more'. Applicants have previously provided the required 'more' which weighs against the obviousness rejection (see the preceding two paragraphs). Applicants note that the Examiner fails to rebut applicants arguments against the combination and improperly fails to address applicants' traversal, even though applicants expressly previously requested that the Examiner identify every element of Tavallaei which is proposed to be modified and the textual or other basis which suggests making such modification.

The Examiner proposes **seven** modifications to the Tavallaei reference. Namely, the Examiner proposes 1) modifying the ASIC 28 in Tavallaei to be an I/O hub; 2) connecting the ASIC 28 to multiple PCI hubs; 3) adding multiple COPICs 312 to Tavallaei; 4) cross-connecting the COPICs 312 with the local APICs 12 in Tavallaei; 5) cross-connecting the COPICs 312 with an I/O hub in Tavallaei; 6) adding a second I/O hub to Tavallaei; and 7) modifying the local APIC 14 in Tavallaei to be coupled to four microprocessors. The

purported motivation to make such modifications are, respectively, 'this would allow more PCI devices to be connected', 'it would provide twice as much throughput and maximum bandwidth', 'this would allow the expandablility of more PCI hubs connected', and 'it would reduce traffic on the bus shared between the nodes'. However, each of these proposed modifications is simply pulled out of thin air without any analysis or explanation of the respective bases.

Only for the last proposed modification does the Examiner even provide a citation to a textual basis (citing col. 10, lines 30-35 of Deshpande). However, the Examiner misconstrues the teachings of Deshpande. The cited portion apparently describes an alternative bus arrangement for a multi-node system (e.g. as compared to Fig. 4 of the same reference), but does not provide any motivation to modify a dedicated local APIC of a multi-processor system to support four processors.

Because the secondary references fail to make up for the deficiencies in Tavallaei, and because there is no motivation to combine the references as suggested by the office action, claim 8 is separately patentable over the cited combination of references.

Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,189,065 (Arndt). Claims 13 and 22 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Olarig in view of Arndt. Applicants respectfully traverse these rejections for the following reasons.

Arndt fails to make up for the above noted deficiencies in Tavallaei and Olarig. Accordingly, the office action fails to establish a prima facie case of obviousness. For the Examiner's convenience, the claim language, the Examiner's stated rejection, and the cited portion of Arndt are reproduced below:

Claims 13 and 22	... wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor.
Examiner's rejection	... Arndt discloses redirecting an interrupt to a different processor. Therefore it would have been obvious to combine the teachings of Arndt and [the primary reference] to redirect an interrupt to different processor since ...
Claim 8 Of Arndt	... an offload selector for offloading said interrupt message to a second processor if said first processor is busy servicing another interrupt signal ...

The claim language does not recite 'redirect an interrupt to a different processor'. The claim language recites that the scaleable node controller redirects the interrupt request through the scalability port switch to a different processor. The office action completely fails to address several of the claim recitations, and accordingly fails to establish a prima facie case of obviousness. The Examiner's response to arguments, in numbered paragraph 65, fails to clarify or explain the Examiner's position or answer applicants' previous traversal. In any event, the cited portion of Arndt is silent in regard to these claim recitations.

Because the Arndt fails to make up for the respective deficiencies in Tavallaei and Olarig, and because there is no motivation to combine the references as suggested by the office action, and because the Examiner fails to establish a prima facie case of obviousness, and because the cited portion of Arndt fails to describe that a scalable node controller redirects the interrupt request through a scalability port switch to a different processor, claims 13 and 22 are separately patentable over the cited combination of references.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

July 11, 2005
Date

/Paul E. Steiner/
Paul E. Steiner
Reg. No. 41,326
(703) 633-6830

Intel Americas, Inc., LF3
4030 Lafayette Center Drive